



FFT Cores

FFTs for Communications and Signal Processing



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ATHENA

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Features

- A family of solutions to meet your requirements
- User defined maximum transform length
- Run-time programmable transform length
- User defined input and output precision
- Multiple radices (e.g., 2, 3, 4, 5) available
- Run-time programmable scaling
- I/O flow control

Benefits

- Portable to multiple implementation technologies, including FPGA, structured ASIC, and ASIC
- Multiple products allow the best FFT to be matched to your application
- Offload/replace DSP micro-processors

Applications

- OFDM modems
- LTE-Advanced/4G, LTE, WiMax, UWB
- Digital excision filtering
- Antenna beamsteering
- Instrumentation, signal analysis



Atomic FFT™ Family

Athena delivers high-performance fast Fourier transform (FFT) cores, ready to use for your SoC application. When your advanced communications or signal processing SoC requires dedicated FFT performance, turn to Athena's Atomic FFT family. Atomic FFT blocks enable your application to realize the power, performance, and area advantages of Athena's arithmetic technology in your FFT intensive application and benefit from Athena's experience delivering extreme FFT performance.

All Atomic FFT cores can perform both forward and inverse transforms with run-time programmable scaling and transform lengths and have flow control. Data precision, maximum transform length, and performance are user defined implementation parameters. Atomic FFT cores are available with standard radix 2/4 lengths, and optional multi-radix (e.g., 2, 3, 4, 5) lengths. Optional features such as hardwired or run-time programmable windowing are also available. The Atomic FFT family is summarized in Table 1.

Table 1: FFT Family Members

Model	Description	Latency ^a
BFFT	Radix 2/4 Sequential Block FFT	$N \log N$
BFFT-M	Multi-Radix Sequential Block FFT	$N \log N$
PFFFT	Radix 2/4 Pipelined FFT	N
PFFFT-M	Multi-Radix Pipelined FFT	N
PPFFT	Radix 2/4 Pipelined Parallel FFT	N/L^b
PPFFT-M	Multi-Radix Pipelined Parallel FFT	N/L^b
CUSTOM	Customer-specific FFT implementation	custom

a. Approximate latency in cycles versus transform length N .

b. Parallelism factor L .

Available Deliverables

- Simulation model (Verilog or VHDL)
- Synthesizable RTL (Verilog or VHDL) and scripts
- Targeted, timing closed netlist
- Bit accurate C models
- Verification suite
- Documentation
- Support



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Customized Solutions

If an off-the-shelf FFT product isn't right for your application, Athena can leverage its FFT generators to create a customized solution with the optimum mix of performance, power, and area for your application and implementation technology. Athena has over 20 years of experience delivering advanced signal processing and FFT solutions for FFT-intensive applications in implementation technologies including FPGA, structured ASIC, standard cell ASIC, and even semi-custom. Athena FFTs have been used in applications from LTE communications to satellite navigation to video cross correlation. Athena is ready to help you solve your toughest signal processing design and system integration problems.

Bit Accurate C Language Models

The same IP generation technology used to create FFT products is used to generate bit accurate C language models. Since the C models are derived directly from the implementation, you can be assured of the accuracy of these models. These models are easily integrated into any system-level verification environment.

FPGA and ASIC Ready

Athena designs its IP products for efficient implementation in both FPGA and ASIC technologies. Athena is equipped with an extensive suite of EDA tools for both ASIC *and* FPGA technologies that enables Athena to optimize its products for all manufacturing technologies. This means that Athena can help you meet the most aggressive area, power, and performance requirements in your implementation technology and without costly last minute surprises.

Designed for Easy Integration

As a premier provider of semiconductor IP, Athena always delivers quality and first-time physical design success. To ensure ease of integration Athena goes the distance - by synthesizing *our* IP into *your* target library, in *your* process, with *your* constraints, and delivering a completed core, ready for place and route. Athena standard deliverables include everything you need to integrate our core into your design.

About The Athena Group, Inc.

Based in Gainesville, Florida, Athena innovates breakthrough technologies that achieve the optimum balance of power, performance, and silicon area in a wide range of applications such as network processors, cellular base stations, and satellite receivers. Athena provides patented semiconductor intellectual property (IP) solutions, with products ranging from the market-leading TeraFire® security cores, to Atomic DSP™ cores, and Atomic SDR™ software defined radio cores.

Athena was founded in 1986 and is privately held.

Features

- A family of FFT and cryptography solutions to meet your LTE/WiMax requirements
- User-defined maximum transform length
- Run-time programmable transform length
- Run-time programmable scaling
- User-defined input and output precision
- Multiple radices (e.g., 2, 3, 4, 5)
- I/O flow control

Benefits

- Single source for both FFT and cryptography
- Portable to multiple implementation technologies, including FPGA, structured ASIC, and ASIC
- Multiple products allow the best cores to be matched to your application

Applications

- LTE-Advanced/4G
- LTE, WiMax
- OFDM modems
- Communications



LTE and WiMax Solutions

Athena is your one-stop shop for both high-performance FFTs and cryptography (see page 5) solutions for LTE and WiMax basestation, femto-cell, and mobile terminal designs.

Multi-Radix FFT Solutions for LTE/WiMax

Today's advanced OFDM, OFDMA, and SC-FDMA based communications schemes need the power and performance benefits of dedicated FFT processing. Athena's PFFT and PFFT-M FFTs use a pipelined streaming architecture to minimize latency and maximize throughput. These FFT cores stream one complex input operand and produce one complex result output per cycle – producing an N -point FFT every N -cycles.

Athena's pipelined FFT cores perform both forward and inverse transforms with run-time programmable scaling and run-time programmable transform length. Data precision, maximum transform length, and throughput are customer defined at time of order. Pipelined FFT cores also support composite transform lengths with multiple radices, including 2, 3, 4, and 5, so a single core can perform all FFT types required by LTE, LTE-Advanced, WiMax, and other OFDM-based communications schemes.

A representative PFFT-M multi-radix FFT configuration for LTE/WiMax in 40 nm technology has the following characteristics:

- 180K-gates plus memory using 16-bit precision
- 500 MHz operating frequency
- Radices 2, 3, 4, and 5 for transform lengths up to 4,096 points¹

1. Supported lengths in this *representative* configuration include: 12, 16, 24, 32, 36, 48, 60, 64, 72, 96, 108, 120, 128, 144, 180, 192, 216, 240, 256, 288, 300, 324, 360, 384, 432, 480, 512, 540, 576, 600, 648, 720, 768, 864, 900, 960, 972, 1024, 1080, 1152, 1200, 1296, 1536, 2048, and 4096.

Available Deliverables

- Simulation model (Verilog or VHDL)
- Synthesizable RTL (Verilog or VHDL) and scripts
- Targeted, timing closed netlist
- Bit accurate C models
- Verification suite
- Documentation
- Support

The same PFFT-M multi-radix FFT configuration implemented in Altera Stratix IV with a 75 MHz operating frequency has the following resource requirements:

- 14,900 ALUTs,
- 32 RAMs (M9K), and
- 138 DSPs.

Representative performance examples are shown in Table 1.

Table 1: PFFT/PFFT-M Performance Examples

Transform Length	FIFO Latency ^a	Cycles/Transform	Transforms/sec ^b
256	264	256	1.95M
720	730	720	694K
1024	1034	1024	488K
1536	1548	1536	326K
4096	4108	4096	122K

- a. First-in to first-out latency with no input stalls.
- b. At 500 MHz operating frequency.

Athena’s pipelined FFTs use a streaming flow-through architecture with dedicated unidirectional write and read ports (see Figure 1). Pipelined FFT functions are easily integrated with other function blocks or may be added to your microprocessor-based design as a function-specific accelerator.

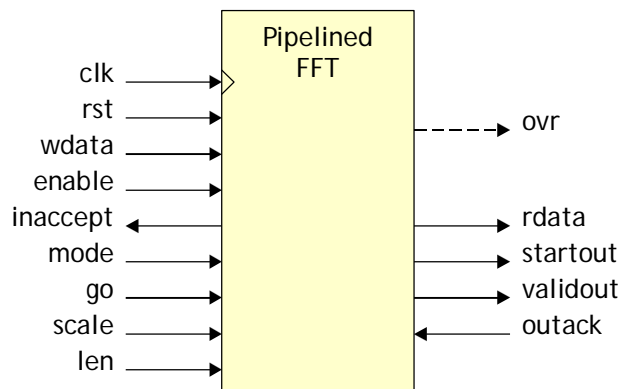


Figure 1: Pipelined FFT Block Interface

Customized Solutions

If an off-the-shelf FFT product is not right for your application, Athena can leverage its FFT generators to create a customized solution with the best possible mix of performance, power, and area for your application and implementation technology. Athena has over 20 years of experience delivering advanced signal processing solutions for FFT-intensive applications in implementation technologies including FPGA, structured

ASIC, standard cell ASIC, and even semi-custom. Athena FFTs have been used in applications from LTE communications to satellite navigation to video cross correlation. Athena is ready to help you solve your toughest signal processing design and system integration problems.

Bit-Accurate C Language Models

The same IP generation technology used to create Athena FFT cores is used to generate Athena's bit-accurate C language models. Since the C models are derived directly from the implementation, you can be assured of the accuracy of these models. These C models are easily integrated into any system-level verification environment.

TeraFire™ Cryptography Solutions for LTE and WiMax

Athena's TeraFire family delivers the hardware security IP you need to get your LTE/WiMax product built. Athena's market-leading public key cryptography accelerators are complemented by the 3GPP ciphers, as well as standard symmetric key cryptography functions for confidentiality, cryptographic hash functions for data integrity, and random number generators for keying. System integration is simplified with optional bus interfaces and a comprehensive software library.

TeraFire cryptography accelerators are the foundation of any security solution. Table 2 summarizes Athena's TeraFire security product family.

Table 2: TeraFire Security Product Family

Model	Description	Performance ^a
EXP-T5200	Public Key (PK) Cryptography Microprocessor ^b	4,900/s ^c 9,800/s ^d
EXP-E5200	Elliptic Curve Cryptography Microprocessor ^b	2,900/s ^e 1,500/s ^f
EXP-F5200	Cryptography Microprocessor (PK) ^b - Optional AES - Optional SHA-1, SHA-2 - Optional RNG	200/s >150 Mbps >150 Mbps
AES-A100	Advanced Encryption Standard (AES)	5.8 Gbps
AES-A200	Standard Performance AES	1.4 Gbps
AES-A300	Compact AES	360 Mbps
SHA1-A100	Secure Hash Algorithm-1 (SHA-1)	2.9 Gbps
SHA2-A100	SHA-1 plus SHA-2 (224/256/384/512) with context change support	3.5 Gbps ^g 5.7 Gbps ^h
SHA2-A200	SHA-1 plus SHA-2 (224/256/384/512) with automatic message padding	3.5 Gbps ^g 5.7 Gbps ^h
SHA2-A300	SHA-1 plus SHA-2 (224/256/384/512) with HMAC and automatic message padding	3.5 Gbps ^g 5.7 Gbps ^h
RNG-A100	SP800-22 True Random Number Generator	250 Mbps
RNG-A200	SP800-90 True Random Number Generator	up to 3.2 Gbps
CAL-A100	Cryptography Application Library (CAL)	N/A
KAS-A100	Kasumi 3GPP Cipher	3.5 Gbps

Table 2: TeraFire Security Product Family (Continued)

Model	Description	Performance ^a
SNOW-A100	SNOW 3GPP Cipher	16 Gbps
3DES-A100	Data Encryption Standard (DES/3DES)	4 Gbps/ 1.3 Gbps
ARC4-A100	ARC4 Stream Cipher	1.3 Gbps
MD5-A100	Message Digest 5 (MD5)	3.75 Gbps
TeraFire AT	Anti Tamper Platform for Secure SoCs	N/A

- a. Performance specified at 500 MHz unless otherwise noted.
- b. TeraFire cryptography microprocessors execute many types of operations; see the respective product briefs for further characterization.
- c. RSA-1024 private key operations at 500 MHz.
- d. Dual-core RSA-1024 private key operations with CRT at 500 MHz.
- e. NIST P-256 point multiply at 500 MHz.
- f. NIST P-384 point multiply at 500 MHz.
- g. Nominal performance for SHA-224/256.
- h. Nominal performance for SHA-384/512.

FPGA and ASIC Ready

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Features

- Streaming pipelined architecture
- User defined maximum transform length
- Run-time programmable transform length
- User defined input and output precision
- Multiple radices available
- Run-time programmable scaling
- I/O flow control

Benefits

- Portable to multiple implementation technologies, including FPGA, structured ASIC, and ASIC

Applications

- Communications
- OFDM modems
- LTE-Advanced/4G
- LTE, WiMax, UWB
- Digital excision filtering
- Antenna beamsteering
- Instrumentation
- Signal analysis



Pipelined FFT

PFFT Radix-2/4 and PFFT-M Multi-Radix FFTs

Athena delivers ultra high-performance fast Fourier transform (FFT) cores, ready to use for your SoC application. When your advanced communications or signal processing SoC requires extreme FFT performance, turn to Athena's Atomic FFT™ blocks. The PFFT and PFFT-M pipelined FFTs use a pipelined streaming architecture to minimize latency and maximize throughput. These FFT implementations are capable of streaming one complex input operand and producing one complex result output per cycle, continuously producing an N -point FFT every N -cycles.

Product Description

Pipelined FFT cores can perform both forward and inverse transforms with run-time programmable scaling and transform lengths. Data precision, maximum transform size, and performance are customer defined at time-of-order. The PFFT supports all power of two transform lengths, and the PFFT-M supports any composite transform length with multiple radices, including 2, 3, 4, and 5. Representative performance examples are shown in Table 1.

Table 1: PFFT/PFFT-M Performance Examples

Transform Length	FIFO Latency ^a	Cycles/Transform	Transforms/sec ^b
256	264	256	1.95M
720 ^c	730	720	694K
1024	1034	1024	488K
1536 ^c	1548	1536	326K
4096	4108	4096	122K

a. First-in to first-out latency with no input stalls.

b. At 500 MHz operating frequency.

c. Requires the PFFT-M.

Available Deliverables

- Simulation model (Verilog or VHDL)
- Synthesizable RTL (Verilog or VHDL) and scripts
- Targeted, timing closed netlist
- Bit accurate C models
- Verification suite
- Documentation
- Support

Athena uses advanced FFT processing techniques to provide transform length agility in the standard pipelined FFT architecture. With transform length agility, power of two transform lengths have a zero cycle delay when switching to other power of two transform lengths. In addition, the delay for switching between other transform lengths is minimal. Athena can also provide pipelined FFT cores without transform length agility for cost sensitive applications.

Athena's pipelined FFTs use a streaming flow-through architecture with dedicated unidirectional write and read ports (see 1). Pipelined FFT functions are easily integrated with other function blocks or may be added to your microprocessor-based design as a function specific accelerator.

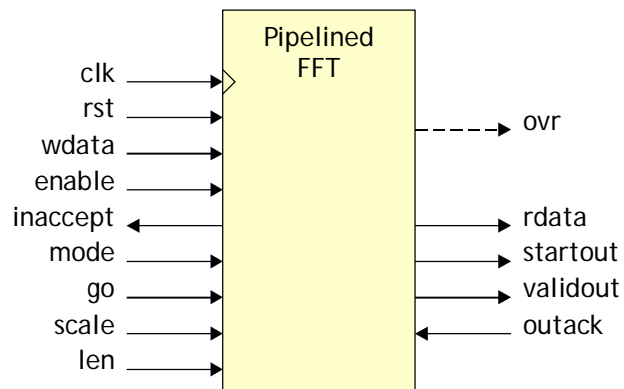


Figure 1: Pipelined FFT Block Interface

Application Proven

Athena has over 20 years of experience delivering advanced signal processing and FFT solutions for FFT-intensive applications in implementation technologies including FPGA, structured ASIC, standard cell ASIC, and even semi-custom. Athena FFTs have been used in applications from LTE communications to satellite navigation to video cross correlation. Whether your application needs an off-the-shelf or customized solution, Athena has the technology and experience to deliver the best FFT for your needs.

FPGA and ASIC Ready

Athena designs its IP products for efficient implementation in both FPGA and ASIC technologies. Athena is equipped with an extensive suite of EDA tools for both ASIC *and* FPGA technologies that enables Athena to optimize its products for all manufacturing technologies. This means that Athena can help you meet the most aggressive area, power, and performance requirements in your implementation technology and without costly last minute surprises.

Designed for Easy Integration

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Features

- Extensive parallel processing for minimum latency, maximum throughput
- User defined maximum transform length
- Run-time programmable transform length
- User defined input and output precision
- Multiple radices available
- Run-time programmable scaling
- User defined parallel data input and output paths
- I/O flow control

Benefits

- Portable to multiple implementation technologies, including FPGA, structured ASIC, and ASIC

Applications

- Communications
- OFDM modems
- LTE-Advanced/4G
- LTE, WiMax, UWB
- Digital excision filtering
- Antenna beamsteering
- Instrumentation
- Signal analysis



Parallel Pipelined FFT

PPFFT Radix-2/4 and PPFFT-M Multi-Radix Parallel Pipelined FFTs

Athena delivers ultra high-performance fast Fourier transform (FFT) cores, ready to use for your SoC application. When your advanced communications or signal processing SoC requires extreme FFT performance, turn to Athena's Atomic FFT™ blocks. The PPFFT parallel pipelined FFT uses a parallel pipelined streaming architecture to minimize latency and maximize throughput. These FFT implementations are capable of streaming two or four complex input operands and producing two or four complex results output per cycle, continuously producing an N -point FFT every $N/2$ -cycles or $N/4$ -cycles.

Product Description

Pipelined FFT cores can perform both forward and inverse transforms with run-time programmable scaling and transform lengths. User defined parallel data input and output paths enable you to match data rates with requirements, without resorting to extreme clock frequencies. Data precision, maximum transform size, and performance are customer defined at time-of-order. The PPFFT supports all power of two transform lengths, and the PPFFT-M supports any composite transform length with multiple radices, including 2, 3, 4, and 5. Representative performance examples are shown in Table 1.

Table 1: PPFFT Performance Examples for $L=2/L=4$ ^a

Transform Length	FIFO Latency ^b		Cycles/Transform		Transforms/sec ^c	
	$L=2$	$L=4$	$L=2$	$L=4$	$L=2$	$L=4$
256	136	72	128	64	3.9M	7.8M
512	266	138	256	128	2.0M	3.9M
720 ^d	370	190	360	180	1.4M	2.8M

Available Deliverables

- Simulation model (Verilog or VHDL)
- Synthesizable RTL (Verilog or VHDL) and scripts
- Targeted, timing closed netlist
- Bit accurate C models
- Verification suite
- Documentation
- Support

Table 1: PFFFT Performance Examples for $L=2/L=4^a$ (Continued)

Transform Length	FIFO Latency ^b		Cycles/Transform		Transforms/sec ^c	
	$L=2$	$L=4$	$L=2$	$L=4$	$L=2$	$L=4$
1024	522	266	512	256	977K	2.0M
1536 ^d	780	396	768	384	651K	1.3M
2048	1036	524	1024	512	488K	977K
4096	2060	1036	2048	1024	244K	488K

- L is the number of input/output operands per cycle.
- First-in to first-out latency with no input stalls.
- At 500 MHz operating frequency.
- Requires the PFFFT-M.

Athena uses advanced FFT processing techniques to provide transform length agility in the standard, parallel pipelined FFT architecture. With transform length agility, power of two transform lengths have a zero cycle delay when switching to other power of two transform lengths. In addition, the delay for switching between other transform lengths is minimal.

Athena's PFFFT uses a streaming flow-through architecture with dedicated unidirectional write and read ports (see Figure 1). Parallel pipelined FFT functions are easily integrated with other function blocks or may be added to your microprocessor-based design as a function specific accelerator.

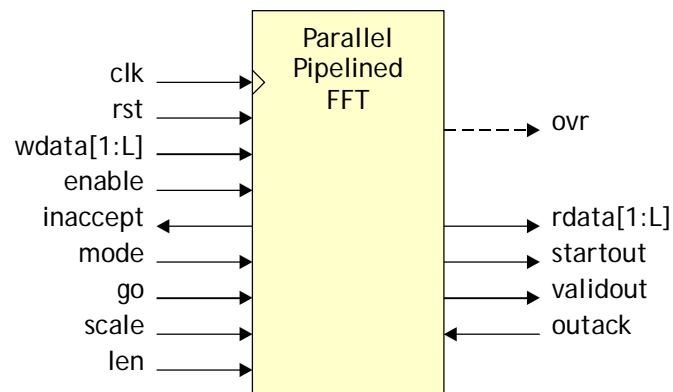


Figure 1: Parallel Pipelined FFT Block Interface

Application Proven

Athena has over 20 years of experience delivering advanced signal processing and FFT solutions for FFT-intensive applications in implementation technologies including FPGA, structured ASIC, standard cell ASIC, and even semi-custom. Athena FFTs have been used in applications from LTE communications to satellite navigation to video cross correlation. Whether your application needs an off-the-shelf or customized solution,

Athena has the technology and experience to deliver the best FFT for your needs.

FPGA and ASIC Ready

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Features

- User defined maximum transform length
- Run-time programmable transform length
- User defined input and output precision
- Multiple radices available
- Run-time programmable fixed scaling
- Automatic block-floating point scaling
- Multiple fixed window options
- Run-time programmable window option
- Real and/or complex windows
- In-place transform pair support
- Digital excision filter option
- In-order or permuted output
- I/O flow control

Benefits

- Feature rich implementation simplifies system-level design
- Block processing core uses single memory for area efficient implementation
- Portable to multiple implementation technologies,



Block FFT

BFFT Radix-2/4 and BFFT-M Multi-Radix FFTs

Athena delivers high-performance fast Fourier transform (FFT) cores, ready to use for your SoC application. When your advanced communications or signal processing SoC requires extreme FFT performance, turn to Athena's Atomic FFT™ blocks. The BFFT and BFFT-M block FFTs use a single dragonfly/butterfly sequential processing architecture to balance performance and implementation resource requirements. The BFFT and BFFT-M are loaded with standard and optional features that make them the most flexible block FFTs available, while the single-memory sequential processing architecture makes the block FFTs extremely area efficient.

Product Description

Block FFT cores can perform both forward and inverse transforms with run-time programmable transform lengths. Run-time programmable fixed and auto scaling simplify dynamic range management. Multiple fixed and run-time programmable window options enable a wide variety of applications, including frequency domain filtering using the in-place transform option. Data precision and maximum transform size are customer defined at time-of-order. The BFFT supports all power of two transform lengths, and the BFFT-M supports any composite transform length with multiple radices, including 2, 3, 4, and 5. Representative performance examples for Block FFTs are shown in Table 1.

Table 1: Block FFT Performance Examples

Transform Length	Cycles/Transform	Transforms/sec ^a
256	1296	386K
512	3092	162K
720 ^b	4340	115K
1024	6164	81K

including FPGA, structured ASIC, and ASIC

Applications

- Communications
- OFDM modems
- LTE-Advanced/4G
- LTE, WiMax, UWB
- Digital excision filtering
- Antenna beamsteering
- Instrumentation
- Signal analysis

Available Deliverables

- Simulation model (Verilog or VHDL)
- Synthesizable RTL (Verilog or VHDL) and scripts
- Targeted, timing closed netlist
- Bit accurate C models
- Verification suite
- Documentation
- Support

Table 1: Block FFT Performance Examples (Continued)

Transform Length	Cycles/Transform	Transforms/sec ^a
1536 ^b	10776	46K
2048	14360	35K
4096	28696	17K

- a. At 500 MHz operating frequency.
- b. Requires the BFFT-M.

Athena’s block FFTs use a flow-through architecture with dedicated uni-directional write and read ports (see 1). Block FFTs are easily integrated with other processor blocks to form a system-level solution or may be added to your microprocessor-based design as a bus attached FFT accelerator, ready to provide greater FFT efficiency than even DSP microprocessors.

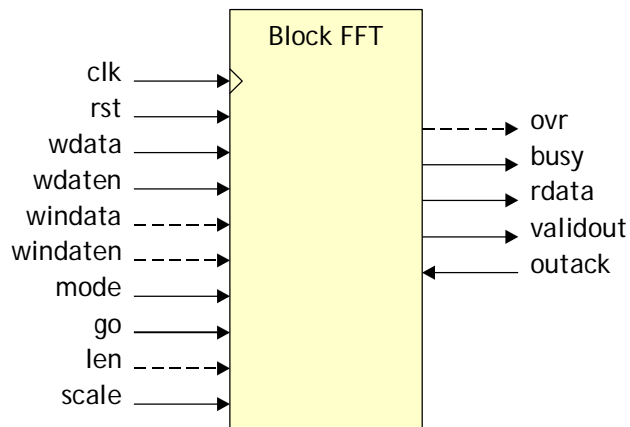


Figure 1: Block FFT Interface

Application Proven

Athena has over 20 years of experience delivering advanced signal processing and FFT solutions for FFT-intensive applications in implementation technologies including FPGA, structured ASIC, standard cell ASIC, and even semi-custom. Athena FFTs have been used in applications from LTE communications to satellite navigation to video cross correlation. Whether your application needs an off-the-shelf or customized solution, Athena has the technology and experience to deliver the best FFT for your needs.

FPGA and ASIC Ready

Athena designs its IP products for efficient implementation in both FPGA and ASIC technologies. Athena is equipped with an extensive suite of EDA tools for both ASIC and FPGA technologies that enables Athena to optimize its products for all manufacturing technologies. This means that Athena can help you meet the most aggressive area, power, and

performance requirements in your implementation technology and without costly last minute surprises.

Designed for Easy Integration

As a premier provider of semiconductor IP, Athena always delivers quality and first-time physical design success. To ensure ease of integration Athena goes the distance - by synthesizing *our* IP into *your* target library, in *your* process, with *your* constraints, and delivering a completed core, ready for place and route. Athena standard deliverables include everything you need to integrate our core into your design.

About The Athena Group, Inc.

Based in Gainesville, Florida, Athena innovates breakthrough technologies that achieve the optimum balance of power, performance, and silicon area in a wide range of applications such as network processors, cellular base stations, and satellite receivers. Athena provides patented semiconductor intellectual property (IP) solutions, with products ranging from the market-leading TeraFire® security cores, to Atomic DSP™ cores, and Atomic SDR™ software defined radio cores.

Athena was founded in 1986 and is privately held.



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Athena IP Delivery and Design Reviews

Assurance of Quality Experience

IP Deliverables

Athena IP deliveries can include the following:

- Timing closed ASIC netlist, targeted for the customer's process, library, clock frequency, and other constraints;
- Synthesizable RTL (VHDL or Verilog) and example synthesis scripts;
- Cycle accurate simulation model (VHDL or Verilog);
- C model;
- Verification suite;
- Software/drivers;
- Documentation; and
- Pre-delivery and post-delivery support.

Depending upon the specific product and customer requirements, optional deliverables under the engagement may include:

- FPGA netlist;
- Preliminary ASIC netlist;
- Physical deliverables; and
- IP customization and/or integration design services.

The Delivery Process

The delivery process is defined by the following milestones:

- Contracting,
- Delivery of optional product views (e.g., FPGA netlist, preliminary ASIC netlist, C model),
- Delivery of final product, and
- Tapeout.

Each milestone is followed by a corresponding review. The purpose of these reviews is to ensure the customer's needs are met at each step in the process. These reviews are:

- Kickoff Review (KR),

-
- Progress Review (PR),
 - Handoff Review (HR), and
 - Final Review (FR).

Kickoff Review (KR)

KR held following execution of a license agreement between Athena and the customer. Topics for KR include:

- Exchange of engineering contacts between the customer's engineering team and Athena's team;
- Implementation parameters (process, library, memories, timing and environmental constraints); and
- Schedule.

Progress Review (PR)

PR is an optional review performed after a preliminary ASIC netlist is delivered. Generally, preliminary netlists are provided for designs with aggressive timing requirements and/or new libraries. The purpose of the PR is to capture any issues that arise from the assessment of the preliminary ASIC netlist so that the identified issues may be addressed prior to production of final deliverables.

Handoff Review (HR)

HR is performed after final deliverables are transmitted to the customer. The purpose of the HR is to review the final deliverables package to ensure that all deliverables meet customer requirements.

Final Review (FR)

FR is performed after the customer completes the physical design based on the final deliverables. The purpose of the FR is to ensure successful outcome, and provides an opportunity give feedback to Athena regarding its products and their delivery.

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