



FFT Cores

FFTs for Communications and Signal Processing



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ATHENA

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Features

- A family of solutions to meet your requirements
- User defined maximum transform length
- Run-time programmable transform length
- User defined input and output precision
- Multiple radices (e.g., 2, 3, 4, 5) available
- Run-time programmable scaling
- I/O flow control

Benefits

- Portable to multiple implementation technologies, including FPGA, structured ASIC, and ASIC
- Multiple products allow the best FFT to be matched to your application
- Offload/replace DSP micro-processors

Applications

- Communications
- OFDM modems
- LTE, WiMax, UWB
- Digital excision filtering
- Antenna beamsteering
- Instrumentation, signal analysis



Atomic FFT Family

Athena delivers high-performance fast Fourier transform (FFT) cores, ready to use for your SoC application. When your advanced communications or signal processing SoC requires dedicated FFT performance, turn to Athena's Atomic FFT family. Atomic FFT blocks enable your application to realize the power, performance, and area advantages of Athena's arithmetic technology in your FFT intensive application, and benefit from Athena's experience delivering extreme FFT performance.

All Atomic FFT cores can perform both forward and inverse transforms with run-time programmable scaling and transform lengths, and have flow control. Data precision, maximum transform length, and performance are user defined implementation parameters. Atomic FFT cores are available with standard radix 2/4 lengths, and optional multi-radix (e.g., 2, 3, 4, 5) lengths. Optional features such as hardwired or run-time programmable windowing are also available. The Atomic FFT family is summarized in Table 1.

Table 1: FFT Family Members

Model	Description	Latency ^a
BFFT	Radix 2/4 Sequential Block FFT	$N \log N$
BFFT-M	Multi-Radix Sequential Block FFT	$N \log N$
BPFFT	Radix 2/4 Block Parallel FFT	$(N/4) \log N$
PFFT	Radix 2/4 Pipelined FFT	N
PFFT-M	Multi-Radix Pipelined FFT	N
PPFFT	Radix 2/4 Pipelined Parallel FFT	N/L^b
2DFFT	2D FFT	N^2
CUSTOM	Customer-specific FFT implementation	<i>custom</i>

a. Approximate latency in cycles versus transform length N .

b. Parallelism factor L .

Available Deliverables

- Simulation model (Verilog or VHDL)
- Synthesizable RTL (Verilog or VHDL) and scripts
- Targeted, timing closed netlist
- Bit accurate C models
- Verification suite
- Documentation
- Support



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Customized Solutions

If an off-the-shelf FFT product isn't right for your application, Athena can leverage its FFT generators to create a customized solution with the best possible mix of performance, power, and area for your application and implementation technology. Athena has over 20 years of experience delivering advanced signal processing and FFT solutions for FFT-intensive applications in implementation technologies including FPGA, structured ASIC, standard cell ASIC, and even semi-custom. Athena FFTs have been used in applications from WiMax communications to satellite navigation to video cross correlation. Athena is ready to help you solve your toughest signal processing design and system integration problems.

Bit Accurate C Language Models

The same IP generation technology used to create FFT products is used to generate bit accurate C language models. Since the C models are derived directly from the implementation, you can be assured of the accuracy of these models. These models are easily integrated into any system-level verification environment.

FPGA and ASIC Ready

Athena designs its IP products for efficient implementation in both FPGA and ASIC technologies. Athena is equipped with an extensive suite of EDA tools for both ASIC *and* FPGA technologies that enables Athena to optimize its products for all manufacturing technologies. This means that Athena can help you meet the most aggressive area, power, and performance requirements in your implementation technology, and without costly last minute surprises.

Designed for Easy Integration

As a premier provider of semiconductor IP, Athena always delivers quality and first-time physical design success. To ensure ease of integration Athena goes the distance - by synthesizing *our* IP into *your* target library, in *your* process, with *your* constraints, and delivering a completed core, ready for place and route. Athena standard deliverables include everything you need to integrate our core into your design.

About The Athena Group, Inc.

Based in Gainesville, Florida, Athena innovates breakthrough technologies that achieve the optimum balance of power, performance, and silicon area in a wide range of applications such as wireless, satellite, and secure communications. Athena provides patented semiconductor intellectual property (IP) solutions, with products ranging from the market-leading TeraFire® security cores, to Atomic DSP™ cores, and Atomic SDR™ software defined radio cores.

Athena was founded in 1986 and is privately held.

Features

- Streaming pipelined architecture
- User defined maximum transform length
- Run-time programmable transform length
- User defined input and output precision
- Multiple radices available
- Run-time programmable scaling
- I/O flow control

Benefits

- Portable to multiple implementation technologies, including FPGA, structured ASIC, and ASIC

Applications

- Communications
- OFDM modems
- LTE, WiMax, UWB
- Digital excision filtering
- Antenna beamsteering
- Instrumentation
- Signal analysis



Pipelined FFT

PFFT Radix-2/4 and PFFT-M Multi-Radix FFTs

Athena delivers ultra high-performance fast Fourier transform (FFT) cores, ready to use for your SoC application. When your advanced communications or signal processing SoC requires extreme FFT performance, turn to Athena's Atomic FFT blocks. The PFFT and PFFT-M pipelined FFTs use a pipelined streaming architecture to minimize latency and maximize throughput. These FFT implementations are capable of streaming one complex input operand and producing one complex result output per cycle, continuously producing an N -point FFT every N -cycles.

Product Description

Pipelined FFT cores can perform both forward and inverse transforms with run-time programmable scaling and transform lengths. Data precision, maximum transform size, and performance are customer defined at time-of-order. Pipelined FFT cores also support composite transform lengths with multiple radices, including 2, 3, 4, and 5. Representative performance examples are shown in Table 1.

Table 1: PFFT/PFFT-M Performance Examples

Transform Length	FIFO Latency ^a	Cycles/Transform	Transforms/sec ^b
256	264	256	1.17M
1024	1034	1024	293K
3072	3084	3072	98K
4096	4108	4096	73K

a. First-in to first-out latency with no input stalls.

b. At 300 MHz operating frequency.

Athena's pipelined FFTs use a streaming flow-through architecture with dedicated unidirectional write and read ports (see Figure 1). Pipelined

Available Deliverables

- Simulation model (Verilog or VHDL)
- Synthesizable RTL (Verilog or VHDL) and scripts
- Targeted, timing closed netlist
- Bit accurate C models
- Verification suite
- Documentation
- Support

FFT functions are easily integrated with other function blocks, or may be added to your microprocessor-based design as a function specific accelerator.

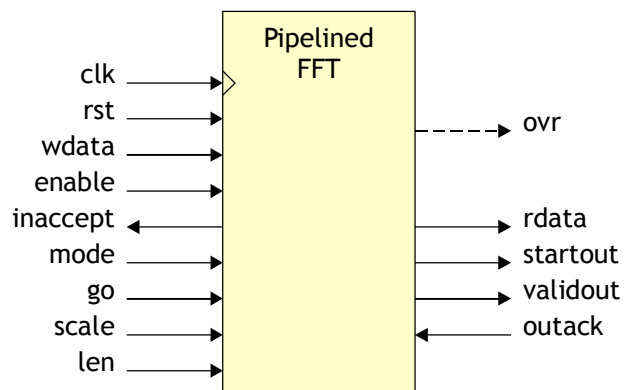


Figure 1: Pipelined FFT Block Interface

Application Proven

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lower power consumption in a broad range of SoC products. Athena's proprietary technology powers leading edge applications such as secure e-commerce, wireless communications, and video compression. In addition to high-value application level solutions, Athena also produces a full line of fundamental DSP functions suitable for SoC integration.

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Features

- Extensive parallel processing for minimum latency, maximum throughput
- User defined maximum transform length
- Run-time programmable transform length
- User defined input and output precision
- Multiple radices available
- Run-time programmable scaling
- User defined parallel data input and output paths
- I/O flow control

Benefits

- Portable to multiple implementation technologies, including FPGA, structured ASIC, and ASIC

Applications

- Communications
- OFDM modems
- LTE, WiMax, UWB
- Digital excision filtering
- Antenna beamsteering
- Instrumentation
- Signal analysis



Parallel Pipelined FFT

PPFFT Radix-2/4 Parallel Pipelined FFTs

Athena delivers ultra high-performance fast Fourier transform (FFT) cores, ready to use for your SoC application. When your advanced communications or signal processing SoC requires extreme FFT performance, turn to Athena's Atomic FFT blocks. The PPFFT parallel pipelined FFT uses a parallel pipelined streaming architecture to minimize latency and maximize throughput. These FFT implementations are capable of streaming two or four complex input operands and producing two or four complex results output per cycle, continuously producing an N -point FFT every $N/2$ -cycles or $N/4$ -cycles.

Product Description

Pipelined FFT cores can perform both forward and inverse transforms with run-time programmable scaling and transform lengths. User defined parallel data input and output paths enable you to match data rates with requirements, without resorting to extreme clock frequencies. Data precision, maximum transform size, and performance are customer defined at time-of-order. Representative performance examples are shown in Table 1.

Table 1: PPFFT Performance Examples for $L=2/L=4$ ^a

Transform Length	FIFO Latency ^b		Cycles/Transform		Transforms/sec ^c	
	$L=2$	$L=4$	$L=2$	$L=4$	$L=2$	$L=4$
256	136	72	128	64	2.3M	4.7M
512	266	138	256	128	1.2M	2.3M
1024	522	266	512	256	586K	1.17M
2048	1036	524	1024	512	293K	586K
4096	2060	1036	2048	1024	146K	293K

- a. L is the number of input/output operands per cycle.
 b. First-in to first-out latency with no input stalls.

Available Deliverables

- Simulation model (Verilog or VHDL)
- Synthesizable RTL (Verilog or VHDL) and scripts
- Targeted, timing closed netlist
- Bit accurate C models
- Verification suite
- Documentation
- Support

c. At 300 MHz operating frequency.

Athena's PPFFT uses a streaming flow-through architecture with dedicated unidirectional write and read ports (see Figure 1). Parallel pipelined FFT functions are easily integrated with other function blocks, or may be added to your microprocessor-based design as a function specific accelerator.

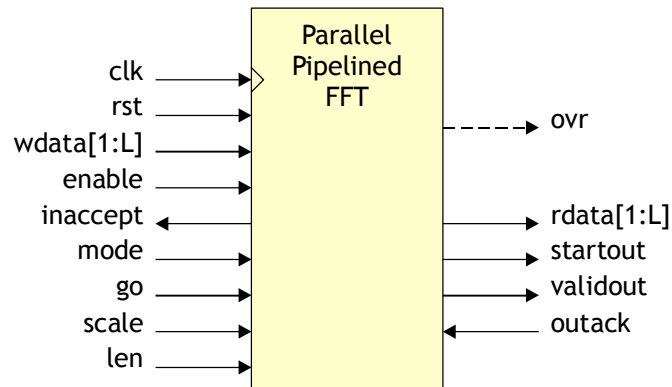


Figure 1: Parallel Pipelined FFT Block Interface

Application Proven

Athena has over 20 years of experience delivering advanced signal processing and FFT solutions for FFT-intensive applications in implementation technologies including FPGA, structured ASIC, standard cell ASIC, and even semi-custom. Athena FFTs have been used in applications from WiMax communications to satellite navigation to video cross correlation. Whether your application needs an off-the-shelf or customized solution, Athena has the technology and experience to deliver the best FFT for your needs.

FPGA and ASIC Ready

Athena designs its IP products for efficient implementation in both FPGA and ASIC technologies. Athena is equipped with an extensive suite of EDA tools for both ASIC *and* FPGA technologies that enables Athena to optimize its products for all manufacturing technologies. This means that Athena can help you meet the most aggressive area, power, and performance requirements in your implementation technology, and without costly last minute surprises.

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Features

- User defined maximum transform length
- Run-time programmable transform length
- User defined input and output precision
- Multiple radices available
- Run-time programmable fixed scaling
- Automatic block-floating point scaling
- Multiple fixed window options
- Run-time programmable window option
- Real and/or complex windows
- In-place transform pair support
- Digital excision filter option
- In-order or permuted output
- I/O flow control

Benefits

- Feature rich implementation simplifies system-level design
- Block processing core uses single memory for area efficient implementation
- Portable to multiple implementation technologies,



Block FFT

BFFT Radix-2/4 and BFFT-M Multi-Radix FFTs

Athena delivers high-performance fast Fourier transform (FFT) cores, ready to use for your SoC application. When your advanced communications or signal processing SoC requires extreme FFT performance, turn to Athena's Atomic FFT blocks. The BFFT and BFFT-M block FFTs use a single dragonfly/butterfly sequential processing architecture to provide balanced performance and implementation resource requirements. The BFFT and BFFT-M are loaded with standard and optional features that make them the most flexible block FFTs available, while the single-memory sequential processing architecture makes the block FFTs extremely area efficient.

Product Description

Block FFT cores can perform both forward and inverse transforms with run-time programmable transform lengths. Run-time programmable fixed and auto scaling simplify dynamic range management. Multiple fixed and run-time programmable window options enable a wide variety of applications, including frequency domain filtering using the in-place transform option. Data precision and maximum transform size are customer defined at time-of-order. Block FFT cores also support composite transform lengths with multiple radices, including 2, 3, 4, and 5. Representative performance examples for Block FFTs are shown in Table 1.

Table 1: Block FFT Performance Examples

Transform Length	Cycles/Transform	Transforms/sec ^a
256	1296	232K
512	3092	97K
1024	6164	48K
1536	10776	28K
2048	14360	21K

including FPGA, structured ASIC, and ASIC

Applications

- Communications
- OFDM modems
- LTE, WiMax, UWB
- Digital excision filtering
- Antenna beamsteering
- Instrumentation
- Signal analysis

Available Deliverables

- Simulation model (Verilog or VHDL)
- Synthesizable RTL (Verilog or VHDL) and scripts
- Targeted, timing closed netlist
- Bit accurate C models
- Verification suite
- Documentation
- Support

Table 1: Block FFT Performance Examples

Transform Length	Cycles/Transform	Transforms/sec ^a
3072	21528	14K
4096	28696	11K

a. At 300 MHz operating frequency.

Athena’s block FFTs use a flow-through architecture with dedicated uni-directional write and read ports (see Figure 1). Block FFTs are easily integrated with other processor blocks to form a system-level solution, or may be added to your microprocessor-based design as a bus attached FFT accelerator, ready to provide greater FFT efficiency than even DSP microprocessors.

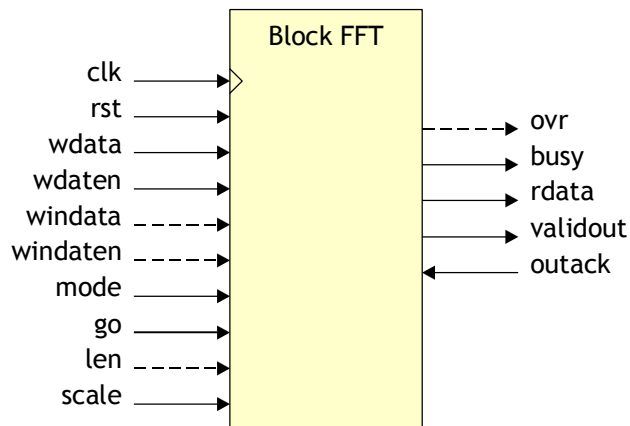


Figure 1: Block FFT Interface

Application Proven

Athena has over 20 years of experience delivering advanced signal processing and FFT solutions for FFT-intensive applications in implementation technologies including FPGA, structured ASIC, standard cell ASIC, and even semi-custom. Athena FFTs have been used in applications from WiMax communications to satellite navigation to video cross correlation. Whether your application needs an off-the-shelf or customized solution, Athena has the technology and experience to deliver the best FFT for your needs.

FPGA and ASIC Ready

Athena designs its IP products for efficient implementation in both FPGA and ASIC technologies. Athena is equipped with an extensive suite of EDA tools for both ASIC and FPGA technologies that enables Athena to optimize its products for all manufacturing technologies. This means that Athena can help you meet the most aggressive area, power, and performance requirements in your implementation technology, and without costly last minute surprises.

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Features

- Extensive parallel processing for minimum latency, maximum throughput
- User defined maximum transform length
- Run-time programmable transform length
- User defined input and output precision
- Multiple radices available
- Run-time programmable scaling
- User defined parallel data input and output paths
- I/O flow control

Benefits

- Extreme computational rates with reasonable clock frequency
- Portable to multiple implementation technologies, including FPGA, structured ASIC, and ASIC
- Offload/replace DSP microprocessors



Block Parallel FFT

BPFFT Radix-2/4 Block Parallel FFTs

Athena delivers ultra high-performance fast Fourier transform (FFT) cores, ready to use for your SoC application. When your advanced communications or signal processing SoC requires extreme FFT performance, turn to Athena's Atomic Fusion FFT blocks. The BPFFT block parallel FFTs use a single dragonfly/butterfly parallel processing architecture to provide balanced performance and implementation resource requirements. The BPFFT provides four times greater performance than block FFTs with a modest increase in resource requirements, making it ideal for applications that perform long transforms.

Product Description

Block parallel FFT cores can perform both forward and inverse transforms with run-time programmable scaling and transform lengths. Data precision and maximum transform size are customer defined at time-of-order. Representative performance examples for block parallel FFTs are shown in Table 1.

Table 1: Block Parallel FFT Performance Examples

Transform Length	Cycles/Transform	Transforms/sec ^a
256	336	893K
1024	1556	193K
4096	7192	42K
16384	32796	9.1K

a. At 300 MHz operating frequency.

Athena's block parallel FFTs use a flow-through architecture with dedicated unidirectional write and read ports (see Figure 1). Block parallel FFTs can accept four operands per clock cycle, and can output four results per clock cycle. With four-operands per cycle parallel I/O, high

Applications

- Communications
- OFDM modems
- LTE, WiMax, UWB
- Digital excision filtering
- Antenna beamsteering
- Instrumentation
- Signal analysis

Available Deliverables

- Simulation model (Verilog or VHDL)
- Synthesizable RTL (Verilog or VHDL) and scripts
- Targeted, timing closed netlist
- Bit accurate C models
- Verification suite
- Documentation
- Support

throughput can be achieved with modest clock frequencies, making block parallel FFTs ideal for applications such as UWB. Block parallel FFTs are easily integrated with other processor blocks to form a system-level solution, or may be added to your microprocessor-based design as a function specific accelerator.

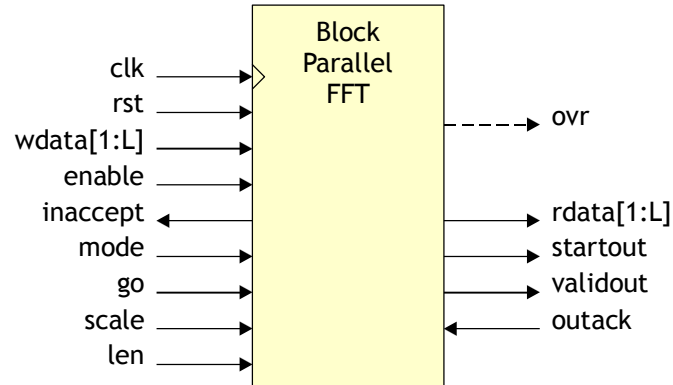


Figure 1: Block Parallel FFT Block Interface

Application Proven

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Features

- Video input preprocessor
- Dynamic filter switching
- Multiple filter per frame processing

Benefits

- High-performance, low cost
- Proven implementation
- Suitable for implementation in FPGA, structured ASIC, or standard cell ASIC
- Enables use of large matched filter databases
- Based on tapeout proven BFFT

Applications

- Automatic target recognition (ATR)
- Positive visual friend or foe identification
- Robotics
- Computer vision
- Surveillance
- Image recognition



AVXCOR

Athena Video Cross Correlator

Athena delivers the world's fastest video cross correlator powered by the world's most efficient Fast Fourier Transform core. Cross correlation systems using matched filters is the methodology of choice for automatic target recognition (ATR), surveillance, and advanced visual identification friend or foe applications. Whatever your application, the Athena AVXCOR delivers unprecedented performance, low power, and a small footprint. Scalable in both performance and image size, the AVXCOR has the flexibility and throughput to tackle nearly any video cross correlation task.

The AVXCOR has the horsepower to generate multiple cross correlation surfaces per video frame, and allows the cross correlation filters to be changed on a frame-by-frame basis, enabling rapid searches of large filter databases. The AVXCOR is ready to power your next generation application with its unbeatable combination of performance and cost.

Product Description

The AVXCOR can be configured for variable frame sizes, throughput rates, and cross correlation surfaces per frame. Starting with 14-bit, 256x256 input at 30 frames per second and eight cross-correlation surfaces per frame, the AVXCOR can be configured to support frame sizes of 1024x1024 or larger, higher frame rates, and even more cross correlation surfaces per frame. Available now in FPGA, the AVXCOR may also be implemented using technologies including structured ASICs as well as standard cell ASICs.

Athena's AVXCOR video cross correlator uses a flow-through architecture with a dedicated video data input and cross correlation surface output, as shown in Figure 1. The AVXCOR includes an input preprocessor that removes the DC component from the input data prior to cross correla-

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- Support

tion processing. This preprocessing stage may be augmented with additional functions such as median filtering, if desired. The Athena BFFT processor, at the heart of the AVXCOR, generates the cross correlation at a throughput rate that can be configured to meet application requirements, and the efficiency of the BFFT allows many of these cores to be implemented in a single device. Frame buffering is performed using commodity synchronous static RAMs to minimize cost and maximize performance.

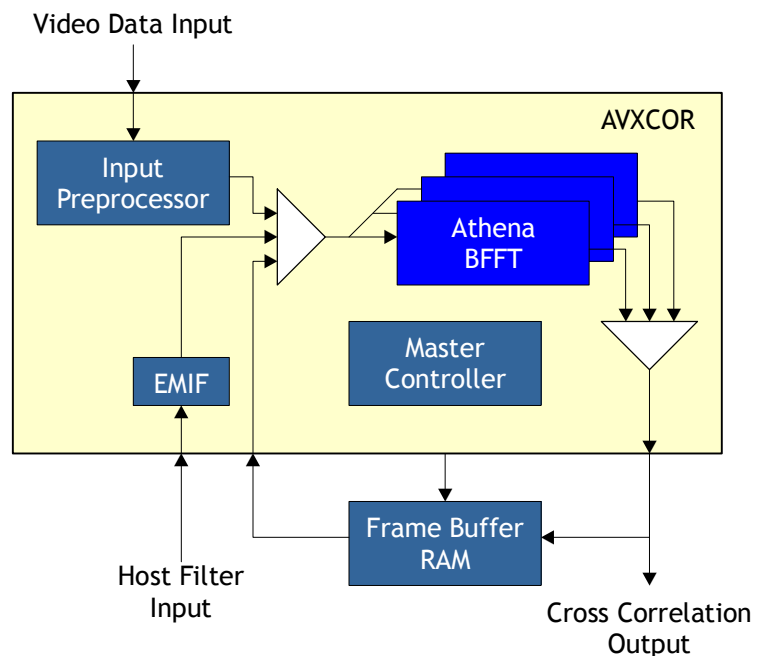


Figure 1: AVXCOR Block Diagram

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Athena designs its IP products for efficient implementation in both FPGA and ASIC technologies. Athena is equipped with an extensive suite of EDA tools for both ASIC and FPGA technologies that enables Athena to optimize its products for all manufacturing technologies. This means that Athena can help you meet the most aggressive area, power, and performance requirements in your implementation technology, and without costly last minute surprises.

Designed for Easy Integration

As a premier provider of semiconductor IP, Athena always delivers quality and first-time physical design success. To ensure ease of integration Athena goes the distance - by synthesizing *our* IP into *your* target library, in *your* process, with *your* constraints, and delivering a completed core, ready for place and route. Athena standard deliverables include everything you need to integrate our core into your design.

About The Athena Group, Inc.

Based in Gainesville, Florida, Athena innovates breakthrough technologies that achieve the optimum balance of power, performance, and silicon area in a wide range of applications such as wireless, satellite, and secure communications. Athena provides patented semiconductor intellectual property (IP) solutions, with products ranging from the market-leading TeraFire® security cores, to Atomic DSP™ cores, and Atomic SDR™ software defined radio cores.

Athena was founded in 1986 and is privately held.



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Athena IP Delivery and Design Reviews

Assurance of Quality Experience

IP Deliverables

Athena IP deliveries can include the following:

- Timing closed ASIC netlist, targeted for the customer's process, library, clock frequency, and other constraints;
- Synthesizable RTL (VHDL or Verilog) and example synthesis scripts;
- Cycle accurate simulation model (VHDL or Verilog);
- C model;
- Verification suite;
- Software/drivers;
- Documentation; and
- Pre-delivery and post-delivery support.

Depending upon the specific product and customer requirements, optional deliverables under the engagement may include:

- FPGA netlist;
- Preliminary ASIC netlist;
- Physical deliverables; and
- IP customization and/or integration design services.

Support Period

Athena provides one year of maintenance and support after final delivery for IP products. Customers may purchase extended maintenance and support at their option.

The Delivery Process

The delivery process is defined by the following milestones:

- Contracting,
- Delivery of optional product views (*e.g.*, FPGA netlist, preliminary ASIC netlist, C model),
- Delivery of final product, and
- Tapeout.

Each milestone is followed by a corresponding review. The purpose of these reviews is to ensure the customer's needs are met at each step in the process. These reviews are:

- Kickoff Review (KR),
- Progress Review (PR),
- Handoff Review (HR), and
- Final Review (FR).

Kickoff Review (KR)

KR held following execution of a license agreement between Athena and the customer. Topics for KR include:

- Exchange of engineering contacts between the customer's engineering team and Athena's team;
- Implementation parameters (process, library, memories, timing and environmental constraints); and
- Schedule.

Progress Review (PR)

PR is an optional review performed after a preliminary ASIC netlist is delivered. Generally, preliminary netlists are provided for designs with aggressive timing requirements and/or new libraries. The purpose of the PR is to capture any issues that arise from the assessment of the preliminary ASIC netlist so that the identified issues may be addressed prior to production of final deliverables.

Handoff Review (HR)

HR is performed after final deliverables are transmitted to the customer. The purpose of the HR is to review the final deliverables package to ensure that all deliverables meet customer requirements.

Final Review (FR)

FR is performed after the customer completes the physical design based on the final deliverables. The purpose of the FR is to ensure successful outcome, and provides an opportunity give feedback to Athena regarding its products and their delivery.

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